REMARKS

By the present amendment, independent claims 3 and 7 have been amended to further clarify the concepts of the present invention. More particularly, claims 3 and 7 have been amended to clarify the step of performing chemical vapor deposition by reciting that the step of depositing an insulation layer includes a CVD process that consists of HDPCVD. Support for these amendments may be found, among other places, in the description at page 9, lines 9 to 20 of the subject specification.

It is submitted that these amendments to the claims are helpful in distinguishing the subject claims over the cited prior art and do not raise new issues which would require further consideration and/or search. In addition, it is submitted that such amendments place the application in better form for appeal by materially reducing or simplifying the issues for appeal. Furthermore, no additional claims are presented without cancelling a corresponding number of finally rejected claims. In view of the above, it is submitted that entry of the above amendments is in order and such is respectfully requested.

In the Office Action, claims 3-4 were rejected under 35 USC § 103(a) as being unpatentable over the patent to Zhang et al in view of the newly cited patent to Park. In making this rejection, it was asserted that the cited Zhang et al patent teaches the method as claimed except for depositing the insulation by performing HDPCVD. The Park patent

was then asserted to teach forming an insulating layer using HDPCVD. It was concluded that it would be obvious to use HDPCVD in the method of the Zhang et al patent since the Park patent teaches HDPCVD provides good burying properties with decreased dishing. Reconsideration of this rejection in view of the above claim amendments and the following comments is respectfully requested.

As mentioned above, independent claim 3 has been amended herein to emphasize that the step of depositing an insulation layer includes a CVD process that consists of HDPCVD. It is submitted that the process as presently claimed in not taught or suggested by the cited patents to Zhang et al and Park whether taken singly or in combination.

As was acknowledged in the Action, the cited Zhang et al patent does not teach a method as claimed where the insulation is deposited by performing HDPCVD. It is submitted that this teaching deficiency is not supplied by the Park patent so as to achieve the presently claimed invention.

In distinct contrast to the present invention, the method of the Park patent includes performing a two-step CVD process consisting of an APCVD operation and an HDPCVD operation as is set forth on col. 3, line 65 to col. 4, line 13. In conducting the APCVD operation, an APCVD layer 33 is formed. The HDPCVD operation is performed after the

APCVD operation so as to deposit HDPCVD layer 34 on the APCVD layer 33. By the two-step CVD processes, a mask aligning trench and an element partitioning trench are filled with the layers 33 and 34 as shown in Fig. 3d. Therefore, although the Park patent teaches performing two-step CVD processes consisting of APCVD and HDPCVD, the Park patent does not teach a CVD process consisting of HDPCVD alone as is presently claimed.

In addition, the Park patent teaches at col. 2, lines 20 to 23 that sole HDPCVD oxide film is unfavorable for filling trenches. Accordingly, a person having ordinary skill in the art would have no motivation to modify any combination of the Park and the Zhang et al patents to achieve the presently claimed invention.

For the reasons stated above, withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 3 and 4 as amended over the cited Zhang et al and Park patents are respectfully requested.

Claim 5 was rejected under 35 USC § 103(a) as being unpatentable over the above patents to Zhang et al and Park in view of the patent to Schoenfeld et al. In making this rejection, it apparently was acknowledged that the cited Zhang et al and Park patents do not specifically teach the use of a rotary grinder in a CMP process, but has asserted that such is taught in the cited secondary patent in connection with a CMP process.

Additionally, claim 6 was rejected under 35 USC § 103(a) as being unpatentable over the above patents to Zhang et al and Park in view of the patent to Kuroi et al. In making this rejection, it apparently was acknowledged that the cited primary Zhang et al and Park patents do not specifically teach (1) use of a silicon substrate, (2) having the insulation formed of silicon oxide and (3) forming a silicon oxide film beneath the silicon nitride film. The patent to Kuroi et al is alleged to supply these teaching deficiencies. Reconsideration of these rejections in view of the above claim amendments and the following comments is respectfully requested.

The above remarks relative to the teaching deficiencies of the Zhang et al and Park patents are reiterated here with regard to this rejection of dependent claims 5 and 6. It is submitted that the Schoenfeld et al and Kuroi et al patents do not supply the above-noted deficiencies. Withdrawal of the rejection therefore is requested.

Claims 7 and 8 were rejected under 35 USC § 103(a) as being unpatentable over the above patents to Zhang et al and Park in view of the patent to Kuroi et al. Similarly to the first rejection, the Zhang et al and Park patents were applied as teaching the method as claimed, but it was acknowledged that the patents do not specifically teach (1) having

the insulation formed of silicon oxide or (2) forming a silicon oxide film beneath the silicon nitride film or layer. The Kuroi et al patent was alleged to supply these deficiencies. Reconsideration of this rejection in view of the above claim amendments and the following comments is respectfully requested.

As mentioned above, independent claim 7 has been amended herein to emphasize that the step of depositing an insulation layer includes a CVD process that consists of HDPCVD. It is submitted that the cited patents to Zhang et al and Park do not teach or suggest, among other things, performing HDPCVD in the manner recited in independent claim 7. It is further submitted that this teaching deficiency is not supplied by the patent to Kuroi et al, among other things, the reasons set forth above.

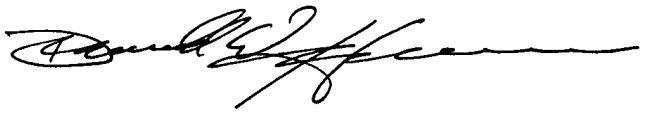
Accordingly, withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 7 and 8 as amended over the cited Zhang et al, Park and Kuroi et al patents are respectfully requested.

In view of the foregoing, it is submitted that the subject application is now in condition for allowance and early notice to that effect is earnestly solicited.

In the event this paper is not timely filed, the undersigned hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



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Marked Up Version of Amendments to Specification and Claims

IN THE CLAIMS:

Please amend claims 3 and 7 as follows:

3. (Twice Amended) A method for manufacturing a semiconductor device, the method comprising:

forming an element partitioning trench and a mask aligning trench in a semiconductor substrate;

depositing an insulation in the element partitioning trench and the mask aligning trench, wherein the step of depositing includes performing a chemical vapor deposition process consisting of ~~by performing~~ high density plasma chemical vapor deposition;

applying a protective mask on the insulation deposited in the element partitioning trench;

etching the insulation deposited in the mask aligning trench to remove some of the insulation; and

flattening an upper surface of the semiconductor substrate.

7. (Twice Amended) A method for manufacturing a semiconductor device, the method comprising the steps of:

forming a silicon oxide film on an upper surface of a semiconductor substrate;

forming a silicon nitride film on the silicon oxide film;

partially removing the silicon nitride film and the silicon oxide film;

forming an element partitioning trench and a mask aligning trench by etching the semiconductor substrate using a residue of the silicon nitride and silicon oxide films as a mask, wherein the element partitioning trench and the mask aligning trench have substantially the same depths;

simultaneously depositing a first layer of insulation and a second layer of insulation in the element partitioning trench and in the mask aligning trench, respectively, wherein the step of simultaneously depositing includes performing a chemical vapor deposition process consisting of ~~by performing~~ high density plasma chemical vapor deposition;

coating the first insulation with a protective mask;

etching the second insulation so that a step is formed between an upper surface of the semiconductor substrate and an upper surface of the second insulation; and

removing the protective mask.